Study of Low Power Array Multiplier for Real Time Applications

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Abstract - Multiplication is one of the essential functions carried out by Arithmetic and Logic Unit. The implementation of multipliers is required in many applications, specifically real time applications such as signal processing analysis, image processing analysis and so on. Designing of the multipliers that requires high speed, low power, less area and with less delay are of significant interest in research area. Numerous attempts have been carried out to reduce the generation of number of partial products in multiplication process. Array multiplier is one such multiplier. High speed integrated circuits can be achieved only with the help of low power consumption. Many arithmetic operations will be performed out using multipliers which is one of the power consuming elements in the digital circuits. The shift and add operations are carried out in the process of multiplication. The performance of multiplier can be improved by optimizing the adder circuit. In this paper, the objective is to build the algorithm for real time application by using array multiplier. The algorithm can be developed using Verilog and the functionalities can be verified through simulation using Xilinx and Chip scope.

Keywords - Multiplication, Array multiplier, Real time applications, Low power, Chip scope.

I. INTRODUCTION

The important parameters that need to be considered while designing the chip are delay, area and the total power consumed by the entire circuit design. These are the parameters which play a significant role in the optimization of digital circuits and systems. Multipliers play a very major role in the designing of real time applications such as performing either signal processing analysis or image processing analysis. The overall delay of the complete circuit depends on the delay of multiplier unit. Intensive study is carried out to decrease the delay of the multiplier unit so that the delay of the entire circuit can be decreased [1]. One of the high speed multiplier that can be considered is Array multiplier. It follows the procedure of generating the partial products. The partial products can be generated by performing the logical AND operation of multiplier and multiplicand bits. The second phase involves with half adders and full adders for the reduction of generated partial products. The third stage involves with performing the addition of two rows with the help of fast carry adders [1]. The advanced technology focuses on reducing the complexity involved in the multiplier unit.

There are several methods carried out to reduce the complexity of the array multipliers. Method 1 involves usage of half adder units [2]. Later stages of improvement involved addition of a single half adder unit at the right most column. This method of implementation of array multiplier unit resulted in the reduction of area. In the later stages of advancement the half and full adders are substituted with Exclusive OR and its complement based 5:2, 4:2 and 3:2 compressors. This implementation reduced the overall delay of the multiplier unit. The switching power can be reduced by including gate level power estimator [5].The partial products will be reordered in such a way that reduces the transitions which in turn results in reduction of power [5]. The architecture design can be done in such a way so that it should be able to minimize the large flow of current along with the transitions occurring in the circuit.

The proposed algorithm implementation consists of replacing the full adder units with modified full adders which are required to generate the partial products in the array multiplier. When compared to the current methods, the proposed method includes the modified full adder circuit using multiplexers which in turn help in the reduction of power along with less area and improving the delay of circuit.

II. PROPOSED ALGORITHM

The algorithm can be implemented using the various blocks. The various blocks consist of Array multiplier, Full adder and Multiplexer based Full adder. The explanation of the various blocks is as follows.

- Array Multiplier: Array multiplier is one of the combinational circuits which consist of half adders and full adders. The composition of the array multiplier can be done as shown in the figure. The architecture of the array multiplier is shown in the figure 1. In an array multiplier, any of the two binary numbers can be considered such as A and B, which will be of m and n bits respectively. The addition operation can be performed which results in producing the

sum bits. These sum bits can be generated parallel by the logical AND gates. The sub blocks in this array multiplier includes n x n multipliers consisting of n(n-2) full adders, n half-adders and n2 logical AND gates.

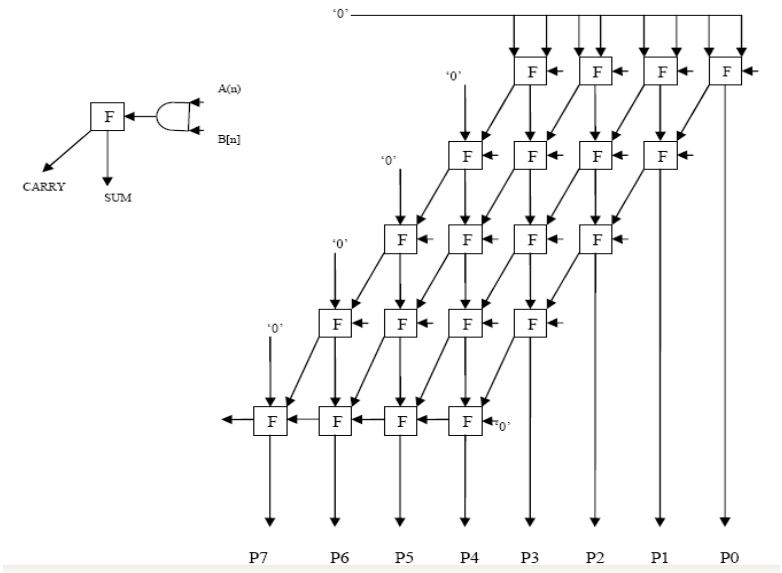

Fig. 1 Architecture of Array Multiplier

- Full adder: The Full adder is a combinational circuit which accepts three inputs and provides the two outputs sum and carry. The hardware requirement in terms of full adder is shown in the figure 2. The Full adder circuit can be designed using 4:1 MUX as shown in the figure 3.

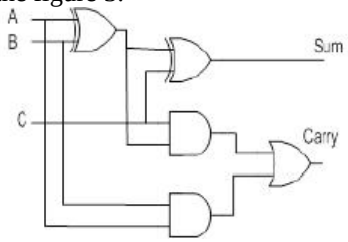

Fig. 2 Full Adder

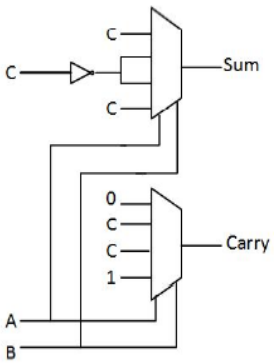

Fig. 3 Full Adder circuit using 4:1 MUX

- Conventional Full Adder: The requirement of full adders in the stage of reduction in the traditional array multiplier is very essential. As seen in the figure 2 the full adder circuit requires two Exclusive OR gates which consumes more amount of power in case of full adder. Hence the delay of two Exclusive OR gates needs to be considered. The path to calculate the sum using one Exclusive OR gate, and to calculate the carry, one logical AND gate and one logical OR gate forms the major path.
- Full Adder using MUX: In order to decrease the power, the conventional full adder which can be used in the reduction phase of array multiplier can be substituted by a modified full adder. As shown in the figure 3 the

implementation of the full adder circuit can be done using 4:1 Multiplexer. The power can be decreased in the array multiplier by implementing full adder circuit with the help of 4:1 MUX. But it is necessary to implement the 4:1 Multiplexer with the help of three such 2:1 Multiplexers. The crucial path delay can be calculated with the help of NOT gate+2 MUX.

- Modified Full Adder: The full adder can be modified as shown in the figure 4. The structure of modified full adder includes 2:1 Multiplexers and an Exclusive OR gate. In this structure, there is a usage of single XOR gate which is substituted by a MUX block so that the overcritical delay with respect to the gate can be reduced. The delay for this circuit can be calculated with the help of XOR gate + MUX.

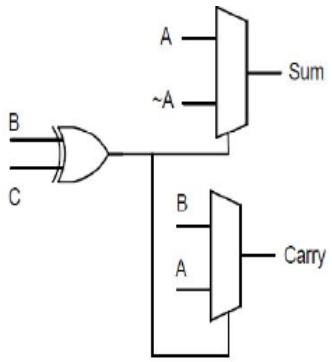

Fig. 4 Modified Full Adder

As seen in the above figure XOR gate output can be used as a select line. Since Exclusive OR gate consumes additional power in the conventional full adder, by reducing the XOR gate in the modified full adder circuit the power consumption can be reduced. The modified FA circuit can be further used in the array multiplier reduction stage to validate its efficiency. The method of operation of the modified FA circuit is as follows.

1) If the inputs B and C are either logic zero or logic one, then the output can be considered as sum=A
2) If either of the inputs B or C is logic one & the other input is logic zero, then the output can be considered as sum=A
3) If both of the inputs B and C are logic zero or logic one, then the output can be considered as carry=B
4) If either of the input B or C is logic one &the other input is logic zero, then the output can be considered as carry=A .

Once if the power consumption in the array multiplier can be reduced with the help of this proposed full adder circuit. It can be further used in the real time applications such as signal processing analysis, image processing analysis and so on.

III. CONCLUSION

This paper discusses about the analysis of power required to model the modified full adder circuit using multiplexers and Exclusive OR gate. The array multiplier can be built using this modified full adder circuit rather than conventional full adder circuit. Hence the power reduction can be achieved in the array multiplier. Further it can be used in any of the real time applications. The algorithm can be developed using Verilog and the functionalities can be verified through simulation using Xilinx and Chip scope.

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