High Performance Reversible Vedic Multiplier using Cadence 45nm Technology

Dr. T.Prabakaran[1], Mr.R.Arun Sekar[2]

[1]Professor, Department of CSE, MREC (A), Secunderabad.
[2]Research scholar, Anna University,Chennai.
Email: prabaakar.t@gmail.com[1], rarunsekar007@gmail.com[2]

Abstract - Vedic science is an antiquated strategy of Indian arithmetic as it contains 16 Sutras. A fast complex 16 *16 multiplier configuration by utilizing Urdhva Tiryakbhyam sutra is introduced in this paper. By utilizing this sutra the fractional items and entireties are created in one stage which decreases the structure of design in processors. By utilizing this sutra we can diminish the time with high degree when contrast with cluster and corner multiplier. It very well may be actualized in numerous Digital Signal Preparing (DSP) applications, for example, convolution, Fast Fourier Transform (FFT) sifting and in microchips. By utilizing this strategy we diminish the engendering delay in correlation with cluster based design and parallel viper based usage which are most regularly utilized models .The fundamental parameters of this paper is engendering delay and dynamic power utilization were ascertained and found decreased.

Keywords - Wallace tree multiplier, Vedic multiplier (VM), Reversible logic

I. INTRODUCTION

Augmentation is a central capacity in math activities dependent on this tasks, for example, Increase and Accumulate(MAC)and internal item are among a portion of the often utilized Computation Intensive Math Functions(CIAF)currently actualized in numerous Digital Signal Processing(DSP)applications, for example, convolution, Fast Fourier Transform(FFT), separating and in chip in its math and rationale unit. Since augmentation overwhelms the execution time of most DSP calculations, so there is a need of rapid multiplier. Right now, increase time is as yet the predominant factor in deciding the guidance process duration of a DSP chip. The interest for fast preparing has been expanding because of growing PC and flag handling applications. Higher throughput number-crunching tasks are essential to accomplish the coveted execution in numerous ongoing sign and picture handling applications. One of the key number-crunching activities in such applications is augmentation and the advancement of quick multiplier circuit has been a subject of enthusiasm over decades. Decreasing the time postponement and power utilization are exceptionally fundamental necessities for some applications. This work presents diverse multiplier models. In this paper a straightforward 16 bit advanced multiplier is proposed which depends on Urdhva Tiryakbhyam (Vertically and Crosswise) Sutra of the Vedic Math's. Two parallel numbers (16-bit each) are increased with this Sutra. The primary idea of this paper is that the control utilization of the circuit and spread postponement of the proposed design. Cluster multiplier, Wallace Multiplier is a portion of the standard methodologies utilized in execution of parallel multiplier which are appropriate for VLSI execution.

Section II describes the Wallace multiplier; Section III describes the basic methodology of Vedic multiplication technique. Section IV describes the proposed Reversible multiplier architecture based on Vedic multiplication. Section V describes the design and implementation of reversible Vedic multiplier module by using Cadence 45 nm technology. Section VI comprises of Result and Discussion for the proposed reversible Vedic multiplier.

II. WALLACE MULTIPLIER

Eminent quick multipliers are Wallace multiplier [1,2] which uses carry save adders to decrease N-sections of fragmented things to two line lattice. The carry save adders are standard full adders whose carry are not related, with the objective that three words are taken in and two words are yield. The Wallace multiplier uses half adders and full adders in their decrease arrange. Here a balanced framework is shown that altogether lessens the half adders. In Wallace multiplier, in the second step of decrease the Wallace approach uses a couple of periods of full adders and half adders as carry save adders. In the Wallace multiplier the incomplete item decrease arrange uses carry save adder. The quantity of full adders and half adders used are 50 and 20 individually. Four phases are required for

decrease. In the middle of the road stages and the last carry propagate phase of standard Wallace tree multiplier, the Carry propagate adder is associated.

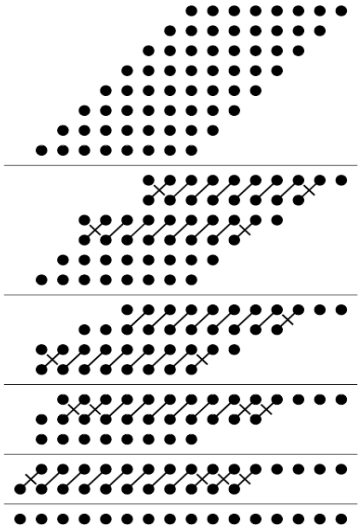

Fig. 1 Schematic of Wallace multiplier

III. VEDIC MATHEMATICS

The utilization of Vedic science is to decreases the regular figuring's in traditional science to exceptionally basic one. Since the Vedic formulae are asserted to be founded on the normal standards on which the human mind works. Vedic Mathematics is a procedure of number juggling decides that permit more effective speed execution. It additionally gives some viable calculations which can be connected to different parts of designing, for example, registering.

A. Urdhva Tiryakbhyam Sutra

The proposed Vedic multiplier [3] depends on the "Urdhva Tiryagbhyam" sutra. These Sutras have been customarily utilized for the augmentation of two numbers in the decimal number framework. In this work, we apply similar plans to the parallel number framework to make the proposed calculation good with the computerized equipment. It is a general augmentation equation relevant to all instances of duplication. It actually signifies "Vertically and Crosswise". It depends on a novel idea through which the age of every single fractional item should be possible with the simultaneous expansion of these incomplete items. The calculation can be summed up for n x n bit number. Since the incomplete items and their wholes are ascertained in parallel and the multiplier is free of the clock recurrence of the processor. Because of its normal structure, it tends to be effectively format in microchips and planners can without much of a stretch bypass these issues to maintain a strategic distance from calamitous gadget disappointments. The preparing intensity of multiplier can without much of a stretch be expanded by expanding the info and yield information transport widths since it has an all in all ordinary structure. Because of its customary structure, it tends to be effectively design in a silicon chip. The Multiplier dependent on this sutra has the favorable position that as the quantity of bits expands, entryway delay and region increments gradually as contrasted with other customary multipliers.

B. Vedic Multiplier for 2x2 piece Module

The strategy is clarified beneath for two, 2 bit numbers A and B where A = a1a0 and B = b1b0. The minimum noteworthy bits are duplicated which gives the minimum huge piece of the last item (vertical). At that point, the LSB of the multiplicand is duplicated with the following higher piece of the multiplier and included with, the result of LSB of multiplier and next higher piece of the multiplicand (across). The total gives second piece of the last item and the carry is included with the fractional item gotten by increasing the most noteworthy bits to give the total and convey. The whole is the third comparing bit and carry turns into the fourth piece of the last item

$$s0 = a0b0; \quad (1)$$

$$c1s1 = a1b0 + a0b1; \quad (2)$$

$$c2s2 = c1 + a1b1; \quad (3)$$

The last outcome will be c2s2s1s0. This augmentation strategy is appropriate for all the cases. The 2X2 Vedic multiplier module is actualized utilizing four information AND entryways and two half-adders . It is discovered that the equipment engineering of 2x2 piece Vedic multiplier is same as the equipment engineering of 2x2 bit conventional Array Multiplier .Hence it is closed that duplication of 2 bit double numbers by Vedic technique does not made noteworthy impact in enhancement of the multiplier's productivity. Precisely we can express that the aggregate postponement is as it were 2-half adder delays, after conclusive piece items are produced, or, in other words to Array multiplier. So we change over to the usage of 4x4 piece Vedic multiplier which utilizes the 2x2 piece multiplier as a fundamental building square. A similar technique can be reached out for input bits 4 and 8. Be that as it may, for higher no. of bits in info, little alteration is required.

C. Vedic Multiplier for 4x4 bit Module

To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers A3A2A1A0 and B3B2B1B0. As the result of this multiplication would be more than 4 bits, we express it as... R3R2R1R0. Line diagram for multiplication of two 4-bit numbers is shown in Figure 2 which is nothing but the mapping in binary system.

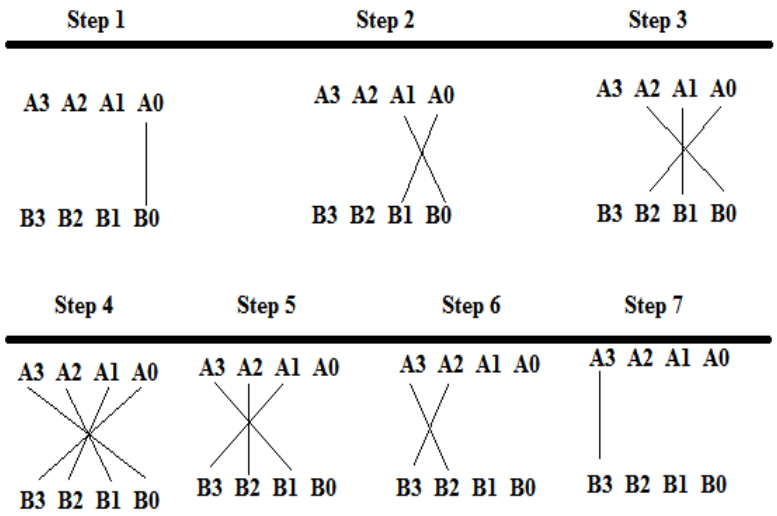

Fig. 2 4X4 bit binary multiplication using Urdhva Tiryakbhyam

Least significant bit R0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier. The process is followed according to the steps shown in Figure 2. Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position.

$$S0 = A0.B0 \quad (4)$$

$$C1S1 = A1B0 + A0B1 \quad (5)$$

$$C2S2 = C1 + A1B1 + A2B0 + A0B2 \quad (6)$$

$$C3S3 = C2 + A3B0 + A0B3 + A1B2 + A2B1 \quad (7)$$

$$C4S4 = C3 + A3B1 + A1B3 + A2B2 \quad (8)$$

$$C5S5 = C4 + A3B2 + A2B3 \quad (9)$$

$$C6S6 = C5 + A3B3 \quad (10)$$

D. Vedic Multiplier for 16x16 bit Module

With four 8x8 multipliers and three 16-bit ripple carry adder, a 16x16 Vedic Multiplier is designed. Here a and b are 16 bit binary numbers. a[15:0]: a15a14a13a12a11a10a9a8a7a6a5a4a3a2a1a0 and b[15:0]:b15b14b13b12b11b10b9b8b7b6b5b4b3b2b1b0.

The first stage has only a single 8 bit Vedic multiplier. The 8 bit Vedic multiplier is built using two 4 bit Vedic multiplier where the 4 bit is built up by two 2 bit Vedic multipliers. Here the output of the first stage is the 16 bit output. The LSB of the output [7:0] is taken directly whereas the MSB [15:8] is fed to the RCA. Segregation of the input bits at the upper stage takes place. The Block diagram of 16 bit Vedic multiplier is shown in the figure 3.Zero padding takes place in one of the RCA to the make the width of the bits equal to the RCA width. Figure 3 clearly explains about the operation of the conventional Vedic multiplier. Here the larger blocks are reduced to half and further reduced to the least level. For example if it is of 8x8 multiplier block, they are reduced to two 4x4 multiplier block and further each 4x4 multiplier block is reduced to two 2x2 multiplier block. Finally the product [31:0] is calculated.

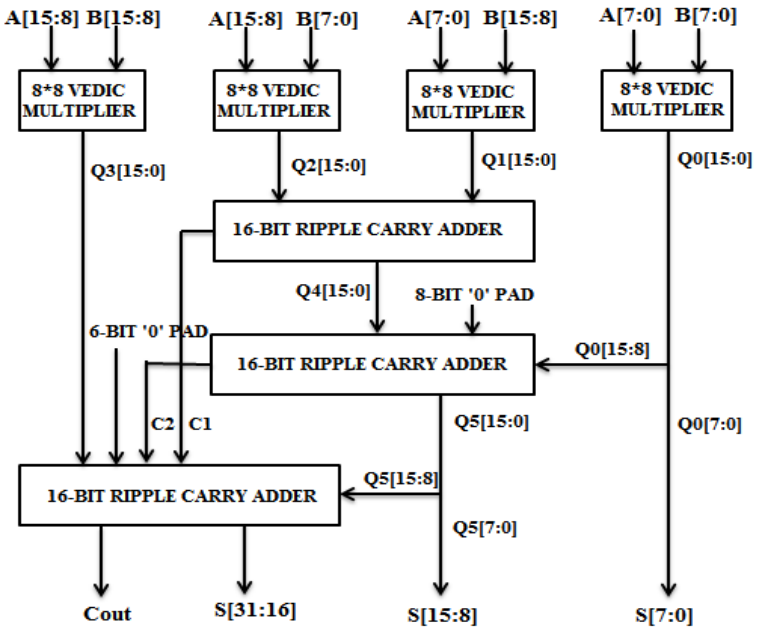

Fig. 3 Block diagram of 16x16 normal Vedic multiplier

IV. REVERSIBLE GATES

A reversible gate is a n input and n output logic. It is said to be one to one mapping phenomenon. The outputs can be easily determined from the inputs meanwhile the inputs can also be obtained from the outputs. Direct fan out is not allowed during the synthesis of reversible circuits since one to many concept is not reversible. Any how we can achieve the fan out in the reversible circuits by utilizing additional gates. While designing the reversible circuit we must keep an eye on using minimum number of reversible logic gates. The complexity and the performance of the circuit are determined by number of factors.

A. BME Gate

BME is a 4*4 reversible gate. It has four inputs and four outputs. The input vector is represented by i(A,B,C,D) and the output vector is represented by o(P,Q,R,S). The output is defined by P = A, Q = AB^C, R = A.D^ C and S = (A'B^C^D).Figure 4 shows the block diagram of BME gate. Figure 5 shows the schematic of BME reversible gate.

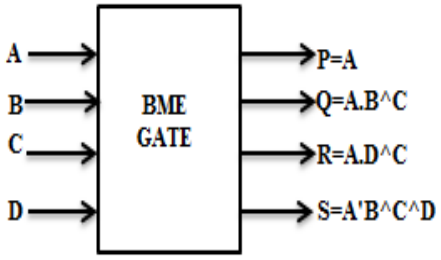

Fig. 4 Block diagram of Reversible BME GATE

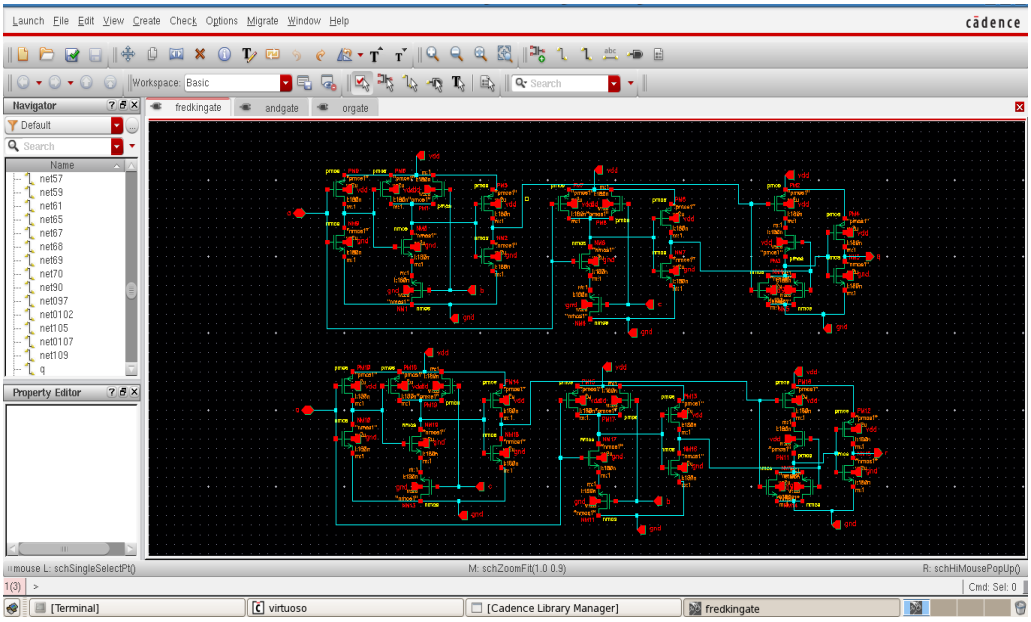

Fig. 5 Schematic of Reversible BME GATE

B. Peres Gate

It is a 3*3 reversible entryway i.e., its 3 sources of info and 3 yields. The illustration of Peres entryway is indicated below in the Figure 6 and Figure 7 shows the schematic of reversible Peres gate by using Cadence tool. The yield is laid out by A, Y=A^B, Z=AB^C. Peres gate has the Quantum cost of five. The truth table of the Peres gate is shown below in the table 1

TABLE 1 TRUTH TABLE OF THE PERES GATE

A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

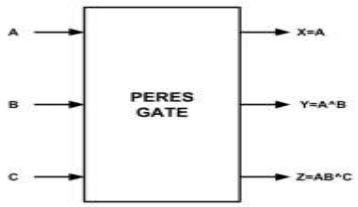

Fig. 6 Block diagram of Reversible Peres GATE

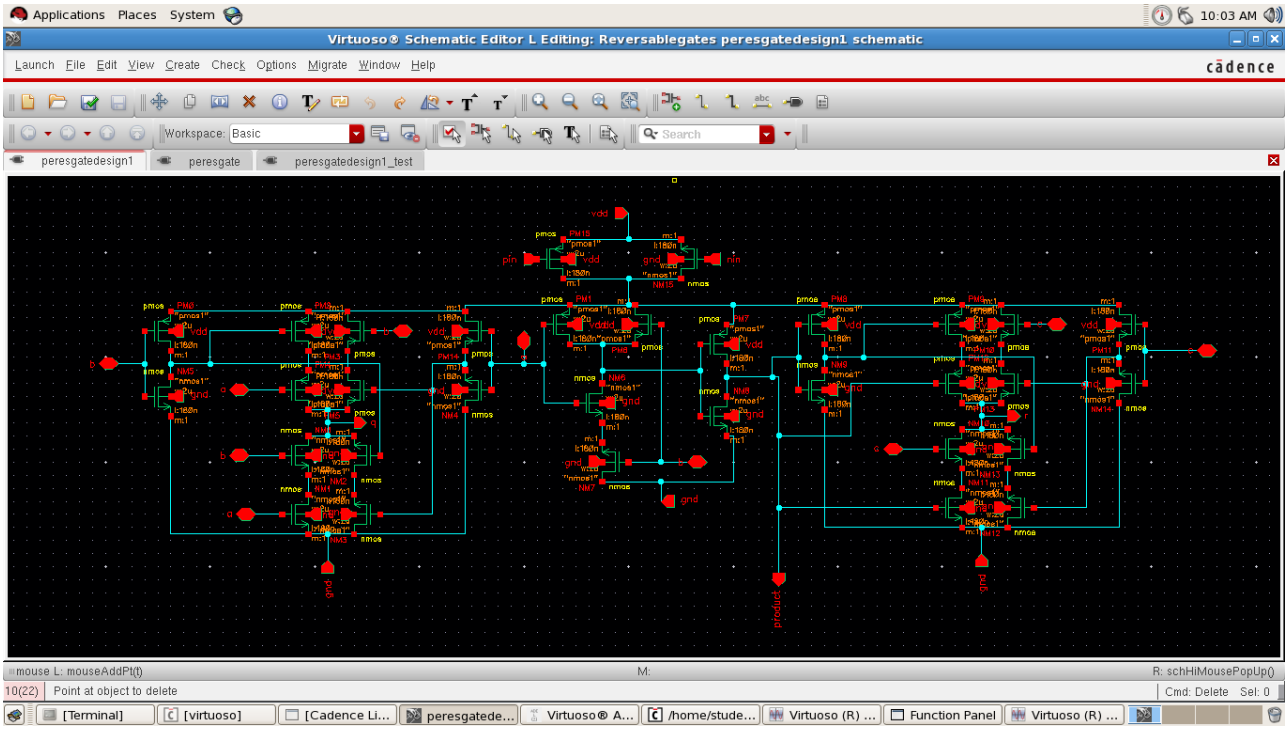

Fig. 7 Schematic of Reversible Peres GATE

V. REVERSIBLE 2*2 VEDIC MULTIPLIER

While designing 4*4 Reversible Vedic multiplier [4-7], it is constructed using two 2*2 Reversible Vedic multiplier. The Block diagram of Reversible 2*2 Vedic multiplier is shown in the Figure 8. Reversible 2*2 multiplier is designed using two BME gate and two PERES gate. The first BME gate produces the sum s0 which is the product of the LSB a0 and b0.Both the two BME gate produces two garbage outputs. One of the outputs of both the BME gate are fed to the PERES gate and the higher order bits of the sum s1, s2 and s3 are generated.

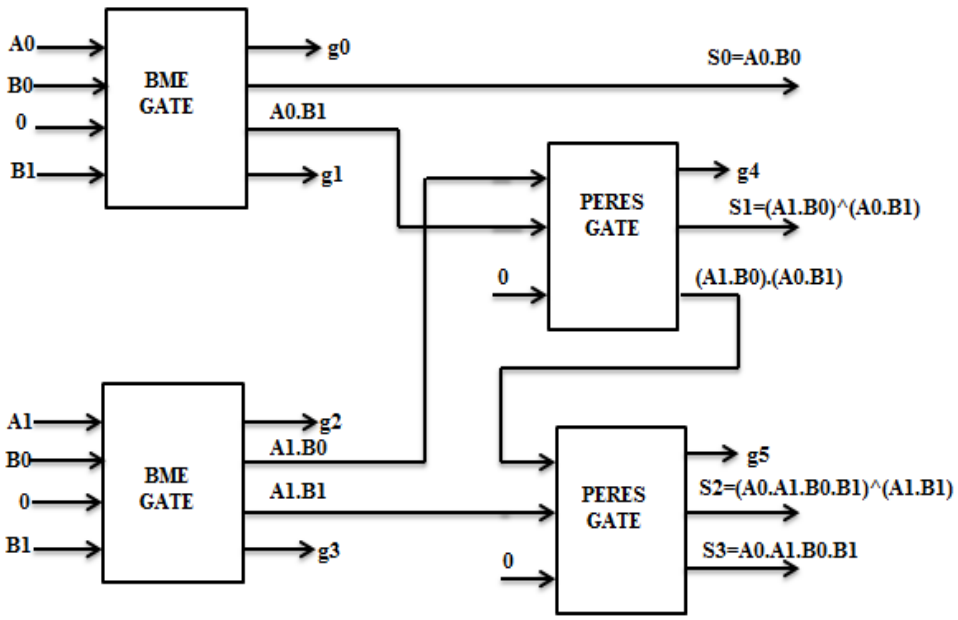

Fig. 8 Block diagram of Reversible 2*2 Vedic multiplier

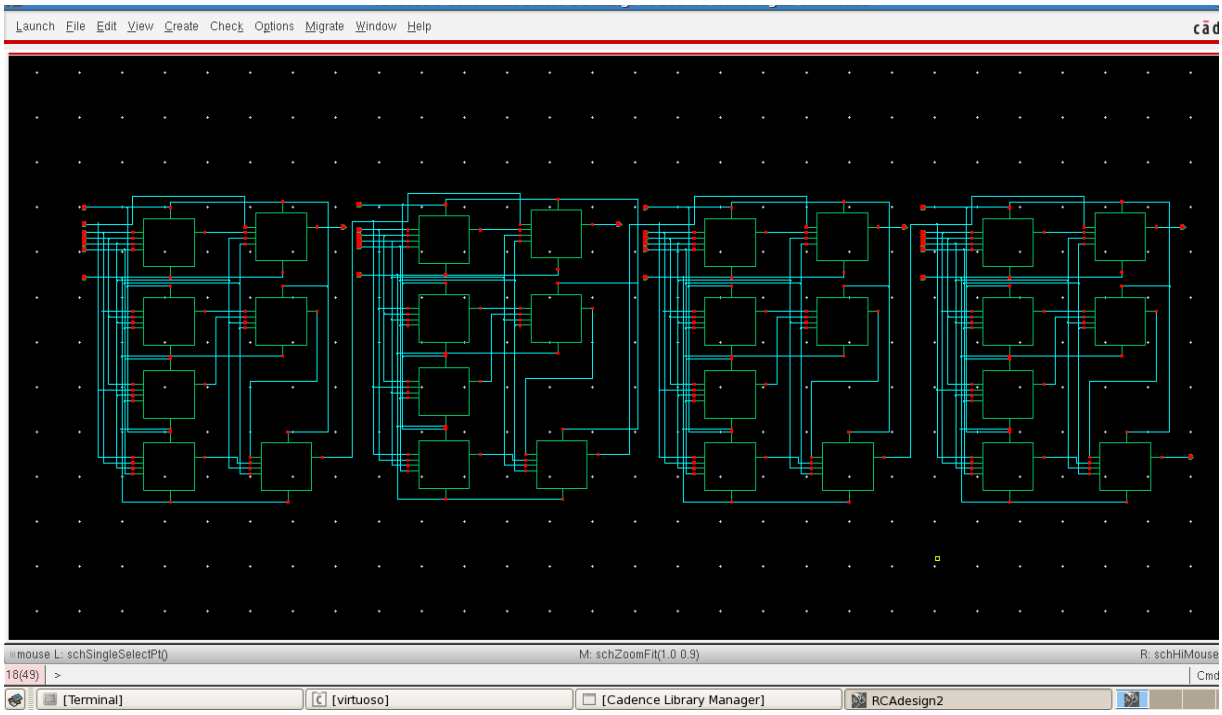

Fig.9 Schematic of Reversible 16*16 Vedic multiplier

Schematic of Reversible 16*16 Vedic multiplier [8-10] is shown in Figure 9.Reversible 16*16Vedic multiplier is designed using multiple stages of 8x8 reversible Vedic multiplier which is constructed from 4x4 Reversible Vedic multiplier and so on. The first stage has only a single 8 bit Reversible Vedic multiplier. The 8 bit Reversible Vedic multiplier is built using two 4 bit Reversible Vedic multiplier where the 4 bit is built up by two 2 bit Reversible Vedic multipliers. Here the output of the first stage is the 16 bit output. The LSB of the output [7:0] is taken directly whereas the MSB [15:8] is fed to the Reversible RCA. Segregation of the input bits at the upper stage takes place. The Schematic of 16 bit Reversible Vedic multiplier is shown in the Figure 9.Zero padding takes place in one of the RCA to the make the width of the bits equal to the RCA width. Here the larger blocks are reduced to half and further reduced to the least level. Finally the product [31:0] is calculated.

VI. RESULTS AND DISCUSSION

TABLE 2: COMPARISON OF DIFFERENT MULTIPLIERS

MULTIPLIER	CELLS	AREA	LEAKAGE POWER (nW)	TOTAL POWER (nW)	DELAY (pS)
WALLACE MULTIPLIER	3562	18732	563901.126	7642414.823	12932
NORMAL VM	736	7125	28905.094	363926.988	6024
REVERSIBLE VM	1945	9844	34628.328	281869.602	5353

Table 2 shows the comparison result of different multipliers. It is generally noted that the Vedic multiplier has lowest delay and low power when compared to other types of multipliers. But when reversible logic is applied to this multiplier, it is seen that the power and delay are further reduced. The delay is reduced by 11.13% and the power is reduced by 22.54%.Figure 10(a) and Figure 10(a) shows the pictorial representation of the comparison result. Simulations are performed using Cadence 45nm technology.

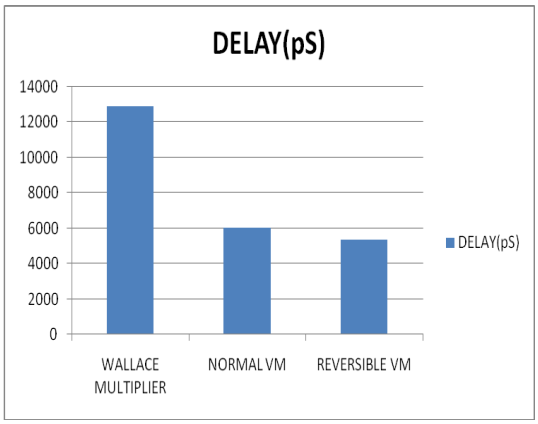

Fig. 10(a) Delay comparison of different multipliers

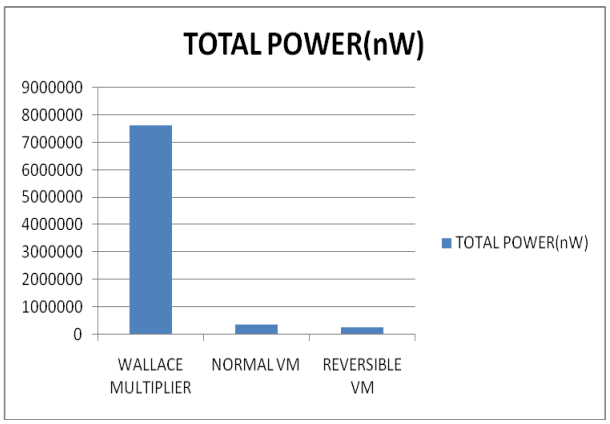

Fig. 10(b) Power comparison of different multipliers

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